Compact all-optical clock and data recovery for variable length asynchronous data packets based on integrated MZI switches

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Abstract: We present and evaluate a compact, all-optical Clock and Data Recovery (CDR) circuit based on integrated Mach Zehnder interferometric switches. Successful operation for short packet-mode traffic of variable length and phase alignment is demonstrated. The acquired clock signal rises within 2 bits and decays within 15 bits, irrespective of packet length and phase. Error-free operation is demonstrated at 10 Gb/s.

OCIS codes: (060.4510) Optical communications; (230.1150) All-optical devices; (250.5980) Semiconductor Optical Amplifiers; (050.2230) Fabry-Perot.

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1. Introduction

The continuing research efforts in photonic integration have led to the development of high-speed, semiconductor based, all-optical switches offering compact size [1] with good potential for their commercial uptake and use in a variety of applications. For this to happen, a substantial cost reduction per optical switch is also a critical issue that needs to be addressed. Efforts are currently under way to achieve the integration of multiple switching elements on a single chip within the European Commission funded IST-MUFINS project [2]. The fabrication of a single photonic chip with multiple elements is expected to considerably reduce the cost per switch by sharing the cost of a single package over many switches, while further reducing size and energy consumption.

The high-speed, bitwise switching capability of all-optical switches makes them ideally suited to a number of point-to-point transmission and networking applications [3,4]. Therefore, all-optical switches emerge as generic devices suitable for the entire routing and processing operation in an all-optical network architecture. One key application in optical network node receivers is clock and data recovery (CDR). Optical packet switched (OPS) network traffic places stringent requirements on clock and data recovery circuits as it consists of variable length (including short) packets. It has been found that 25% of real IP traffic consists of data packets in the 40-44 byte range [5]. Furthermore incoming node packet traffic originates from several sources that are physically separated and change with time. As such, OPS network CDR circuits must be able to operate with data packets that arrive asynchronously in time while at the same time imposing low bandwidth overhead associated with the time needed for clock acquisition. Asynchronous packet-mode operation has been demonstrated at 40 Gb/s with a self-pulsating laser for clock extraction and an ultra-long SOA for regeneration of the incoming data [6]. This approach requires specialized fabrication process for the self-pulsating laser and therefore lacks the potential for large-scale cost reduction, which can be provided by a generic and multifunctional all-optical switch. In the same approach, the recovered clock signal is obtained within 3 ns from the beginning of the data packet and persists phase-locked for more than 10 ns after the packet ends, which corresponds to a few hundreds of bits that must be allowed as guardbands between packets for the clock recovery unit to reset. Asynchronous, short packet CDR was also demonstrated in [7]. The clock recovery circuit consisted of a low-Q, micrometer adjustable bulk Fabry-Pérot etalon with free spectral range chosen at the line rate and followed by an all-optical switch while data recovery was obtained using a second all-optical switch. Both all-optical switches were Ultrafast Nonlinear Interferometers (UNI) constructed from bulk components and used semiconductor optical amplifiers (SOAs). Even though these experiments proved the concept, the CDR circuit was too cumbersome to be considered in a ‘real-life’ packet receiver and has no prospects for integration.

In the present communication, we demonstrate a compact 10 Gb/s CDR circuit that has operational characteristics applicable to OPS networks. It has been built with two generic, integrated, Mach-Zehnder Interferometric (MZI) switches [8] and a fiber Fabry-Pérot filter. The circuit locks within 200 ps and has a decay time of 1.5 ns irrespective of packet length and phase alignment imposing minimal bandwidth penalty. Given that the clock recovery module has been tested at 40 Gb/s [9] and that optical gates have demonstrated operation in the femtosecond regime [10] our CDR is expected to be scalable in terms of operating speed. It is the first time to our knowledge that a CDR circuit capable of operating with asynchronous, variable length, short packets and constructed with integrated MZI gates is being demonstrated. A key advantage of the circuit that can help reduce its cost is that it uses generic, multi-purpose, MZI switches and not one-off, specially designed optical device. Our circuit design and experimental results obtained show the advantages to be expected when single chip, multi-gate integrated arrays become available.

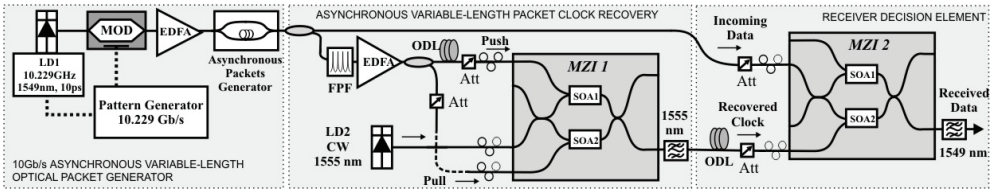

Fig. 1. Experimental setup

2. Experimental Setup

The experimental setup is shown in Fig. 1 and consists of the asynchronous packet flow generator and the CDR circuit comprising the packet clock recovery unit and the decision element. The input signal was generated by a DFB laser diode (LD1) at 1549.2 nm, gain switched at 10.229 GHz to provide 11 ps pulses after linear compression. This pulsetrain was modulated into data packets of variable length containing a 2^7-1 PRBS data pattern, produced by a programmable pattern generator, driving a Ti:$LiNbO_3$ modulator. The data packets entered the asynchronous split-and-combine fiber multiplexer, designed to provide a differential delay of approximately 10 ns between the two optical paths. Fine adjustment of the phase alignment was accomplished using a variable optical delay line inserted in one path of the multiplexer. Synchronous operation could be achieved by disabling one branch of the multiplexer. The generated asynchronous, variable length data packets were then split and inserted into the packet clock recovery module and the decision element. All-optical timing extraction was performed in the packet clock recovery circuit, which employed a low-Q Fiber Fabry-Pérot Filter (FFP) with free spectral range (FSR) equal to the line rate and finesse of 47, as well as an integrated Mach-Zehnder Interferometer (MZI 1) powered by a CW signal at 1555.6 nm (LD 2), operating as a holding beam. The FFP filter acts as a passive optical resonator that extracts the line rate spectral component of the input signal, transforming the data packets into clock packets with intense amplitude modulation and duration similar to the corresponding input, as a result of the exponentially decaying impulse response of the filter. This clock-resembling signal entered the nonlinear gate which acted as a power limiter

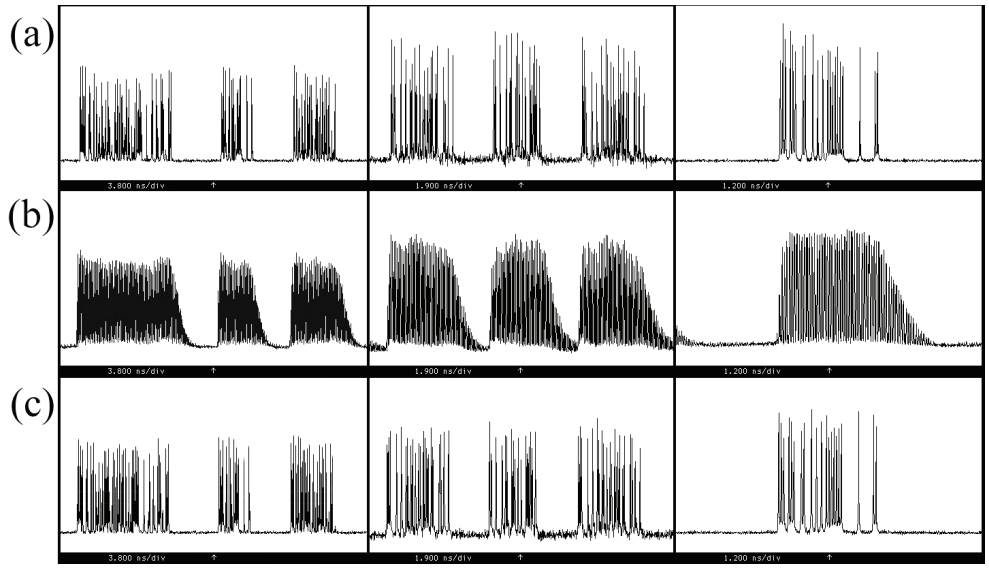

Fig. 2. Pulse traces. First column: synchronous operation (time scale 3.8 ns/div), second column: asynchronous operation (time scale 1.9 ns/div), third column: individual packet (time scale 1.2 ns/div). (a): input signal, (b): recovered clock, (c): recovered signal.

saturated by the CW light. A push-pull configuration was adopted in order to reduce the switching window, thus obtaining clock pulses with 20 ps temporal width. The clock packets were inserted as the control signal in a second integrated Mach-Zehnder Interferometer (MZI 2) constituting the decision element of our CDR. The sampling of the optical packets with their corresponding clock packets leads to the pulse-to-pulse amplitude equalization of the data pulses and their effective retiming. Fine synchronization of the two optical signals was obtained with a variable optical delay line. Both non-linear gates were hybrid integrated MZIs with 1.1 mm SOAs. The footprint of the MZIs was 72 mm × 30 mm and for the FPF 57.2 mm × 14.3 mm.

3. Results and Discussion

The performance of the system was tested for both synchronous and asynchronous operation at 10 Gb/s, with data patterns of different length and phase adjustment. The left column of Fig. 2(a) depicts a typical sequence of three synchronous data packets, containing 116, 40 and 54 bits respectively. Asynchronous operation is demonstrated at the second column of the same figure. Packet length is 40, 30 and 40 bits whereas the first two packets are phase misaligned with respect to the third. The circuit provided the same performance irrespective of phase adjustment and packet length. Fig 2(b) shows the recovered clock packet stream at the output of MZI 1, demonstrating a sharp rise time of only 2 bits and a trailing edge of 15 bits, in close agreement with the theoretical model in [11]. This rise time determines the clock acquisition time of the clock recovery module, whereas the trailing edge specifies the minimum inter-packet guard bands. Both values are proportional to the finesse of the filter and, as a sum, specify the bandwidth overhead imposed by our CDR circuit. The recovered data are shown in Fig. 2(c). The right column of Fig. 2 illustrates the corresponding pulse traces at a smaller time scale, depicting a single data packet. The acquired eyes of the input and recovered data are depicted in the inset of Fig. 3(a) and (b) for the synchronous and asynchronous packet-mode patterns respectively.. The nonlinear transfer function of the gate accounts for the amplitude equalization of the pulses, whereas retiming of the data packets is achieved by triggering the degraded data signal with the extracted, low-jitter clock packets.

The Bit-Error-Rate (BER) performance was tested for both data patterns in synchronous operation, by disabling one branch of the fiber multiplexer. Fig. 3 shows the BER curve for branch 1, exhibiting error-free operation with a negative power penalty. Similar results were obtained for branch 2. The timing jitter performance of the circuit was analyzed by integrating the Single Side Band (SSB) noise spectra of the input, recovered clock and regenerated signal from offset frequency of 1 kHz to 10 MHz from the carrier, as depicted in Fig. 4. The root-mean-square (rms) values were 1.3 ps for the input, 700 fs for the packet clock and 870 fs for

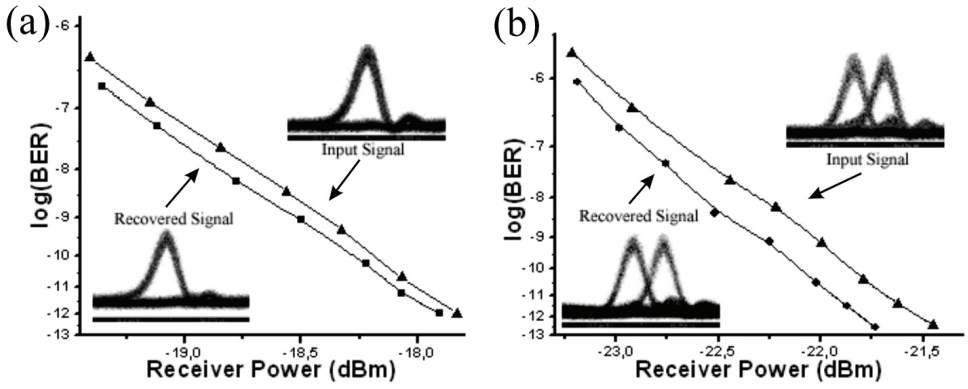

Fig. 3. BER measurements and acquired eye diagrams for the two data patterns used.

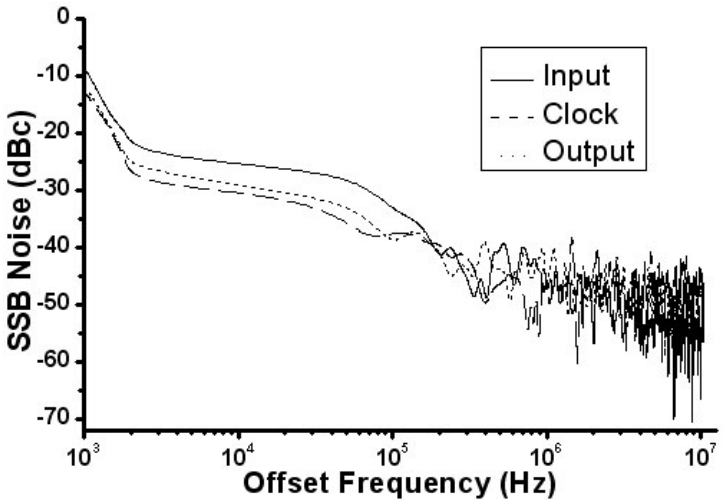

Fig. 4. SSB noise spectra of the input, clock and recovered signal.

the regenerated signal. The FFP filter is centered to the carrier, suppressing the data harmonics, thus reducing the timing jitter of the recovered clock. The switching power and the energy per pulse for MZI 1 were 540 μW for the CW, 22 fJ for the push and 11 fJ for the pull control signal. The pulse energies for MZI 2 were 3 fJ for the packet flow and 4 fJ for the control signal. The clock recovery module provided 300 μW of output power, whereas the decision element required 200 μW for successful operation

4. Conclusion

We have presented a compact all-optical CDR subsystem built with integrated MZIs. Error-free operation of the circuit is demonstrated at 10 Gb/s, obtaining substantial jitter reduction from 1.3 ps to 870 fs. The CDR acquires clock within 2 bits and the total bandwidth penalty in each packet period is only 17 bits, irrespective of packet length and phase alignment, providing high bandwidth utilization and fine granularity to the network. The recovered clock and data remain in the optical domain, permitting possible application of the circuit as a front-end in all-optical nodes for future packet switched networks [12]. Moreover, the fast-locking characteristics and the packet-by-packet operation render this unit convenient for deployment in a TDM Passive Optical Network (PON) for data acquisition at the Central Office nodes [13]. In view of the integration activities in multi-gate arrays [2] circuit cost, size and energy consumption are expected to scale down considerably. In addition, the multi-purpose property of the all-optical switch offer the potential for further cost reduction.

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